B1

6. (Amended) The memory system of claim 5 wherein each channel of the plurality of channels includes a plurality of terminated signal lines.

B2

9. (Twice Amended) The memory system of claim 1 further including a plurality of sideband signals coupled between the buffer device and the memory controller.

B3

39. (Amended) The memory device of claim 10 wherein the first buffer device further includes a write buffer, coupled to the first interface of the first buffer device, to hold data to be provided to at least one memory device of the first plurality of memory devices.

B4

45. (Amended) The memory system of claim 23 further including first termination disposed on the buffer device to terminate the second connection of the first point-to-point link.

46. (Amended) The memory system of claim 45 further including second termination disposed on the controller device to terminate the first connection of the first point-to-point link.